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EXAMINER	
JONES, ERIC W	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/584,052	POCAS ET AL.	
	Examiner	Art Unit	
	ERIC W. JONES	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-64* is/are pending in the application.

4a) Of the above claim(s) *20-26,46-52 and 58-64* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,27-45 and 53-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/23/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claims 8 and 34 are objected to because of the following informalities: Claim 8, line 5; and Claim 34, line 3 state 'le silicon – Germanium'. For examination purposes, it is interpreted that line 5 of claim 8; and line 3 of claim 34 read 'Silicon – Germanium'. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 8-10, 12, 15 and 16; 27, 28, 34-36, 38, 41 and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Kub et al (US 6,274,892 B1).

Re claim 1, Kub et al disclose in FIGS. 1-6 a sealing processing for two wafers made of semiconducting materials, comprising:

- a step for implantation of metallic species (92 in FIG. 2; column 6, lines 66-67 and column 7, lines 1-5) in at least the first wafer (80 in FIG. 2; column 6, lines 66-67 and column 7, lines 1-5),

- a step for assembly of the first and second wafer (95 in FIG. 6; column 9, lines 23-61)

by molecular (hydrophobic) bonding (column 9, lines 37-61),

- a step for formation of metallic compounds (PtSi interface 103 in FIG. 6; column 9, lines 32-37), alloys between the implanted metallic species and the semiconducting materials of the two wafers (after the two wafers are bonded, they are annealed which in turn causes the Pt metallic species to diffuse and react with the silicon substrate (wafer) to form the metallic compound PtSi; column 6, lines 66-67 and column 7, lines 1-5 and 53-60).

Re claim 2, Kub et al disclose the formation step of the metallic compounds resulting from a heat treatment at a temperature equal at least to the formation temperature of the said compounds. (800^{o} C or less; column 6, lines 66-67 and column 7, lines 1-5 and 53-60)

Re claim 8, Kub et al disclose each of the wafers being made from a material chosen from among silicon, gallium arsenide (GaAs), SiC (silicon carbide), InP (Indium phosphide), Germanium (Ge), Silicon - Germanium (SiGe). (column 8, lines 40-47)

Re claim 9, Kub et al disclose the implanted species being platinum or transition metals. (column 5, lines 23-30, column 6, lines 66-67 and column 7, lines 1-5)

Re claim 10, Kub et al disclose at least one of the wafers being heterostructure, for example of the SOI type. (column 18, lines 52-59)

Re claim 12, Kub et al disclose at least one of the wafers being a debondable structure. (wafers 80 and 95 are both debondable since the are bonded by low energy molecular (hydrophobic) bonding as is disclosed by the applicant; column 9, lines 37-61)

Re claim 15, Kub et al disclose at least one of the wafers comprising at least one circuit or circuits layer, on or close to its face to be assembled. (wafers 80 and 95 both comprise N-type base layers 82 and 96 on their faces to be assembled; column 9, lines 10-37)

Re claim 16, Kub et al disclose the implantation step of metallic species (Pt lifetime killing) being done through a mask (photolithographic or metal) to obtain local implantation zones (column 7, lines 9-20).

Re claim 27, Kub et al disclose in FIGS. 1-9 a sealing processing for two wafers made of semiconducting materials, comprising:

- a step for implantation of metallic species (92 in FIG. 2; column 6, lines 66-67 and column 7, lines 1-5) in at least the first wafer (80 in FIG. 2; column 6, lines 66-67 and column 7, lines 1-5),
- a step for assembly of the first and second wafer (95 in FIG. 6; column 9, lines 23-61) by molecular (hydrophobic) bonding (column 9, lines 37-61),
- a step for formation of metallic compounds (PtSi interface 103 in FIG. 6; column 9, lines 32-37), alloys between the implanted metallic species and the semiconducting materials of the two wafers (after the two wafers are bonded, they are annealed which in turn causes the Pt metallic species to diffuse and react with the silicon substrate (wafer) to form the metallic compound PtSi; column 6, lines 66-67 and column 7, lines 1-5 and 53-60), said metallic compound forming a resistive contact between the two wafers, at the assembly interface (FIGS. 7-9; column 9, lines 62-67 and column 10, lines 1-25).

Re claim 28, Kub et al disclose the formation step of the metallic compounds resulting from a heat treatment at a temperature equal at least to the formation temperature of the said compounds. (800° C or less; column 6, lines 66-67 and column 7, lines 1-5 and 53-60)

Re claim 34, Kub et al disclose each of the wafers being made from a material chosen from among silicon, gallium arsenide (GaAs), SiC (silicon carbide), InP (Indium phosphide), Germanium (Ge), Silicon - Germanium (SiGe). (column 8, lines 40-47)

Re claim 35, Kub et al disclose the implanted species being platinum or transition metals. (column 5, lines 23-30, column 6, lines 66-67 and column 7, lines 1-5)

Re claim 36, Kub et al disclose at least one of the wafers being heterostructure, for example of the SOI type. (column 18, lines 52-59)

Re claim 38, Kub et al disclose at least one of the wafers being a debondable structure. (wafers 80 and 95 are both debondable since the are bonded by low energy molecular (hydrophobic) bonding as is disclosed by the applicant; column 9, lines 37-61)

Re claim 41, Kub et al disclose at least one of the wafers comprising at least one circuit or circuits layer, on or close to its face to be assembled. (wafers 80 and 95 both comprise N-type base layers 82 and 96 on their faces to be assembled; column 9, lines 10-37)

Re claim 42, Kub et al disclose the implantation step of metallic species (Pt lifetime killing) being done through a mask (photolithographic or metal) to obtain local implantation zones (column 7, lines 9-20).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 3 and 29; and 11 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kub et al.

Re claims 3 and 29, Kub et al disclose the metallic species (Pt) being implanted at a depth (Rp) of 10 microns under the surface of the implanted wafer. (column 2, lines 65-67, column 3, lines 1-8, column 6, lines 66-67 and column 7, lines 1-5)

Kub et al fail to disclose the metallic species being implanted at a depth (Rp) of between 5 nm and 20 nm under the surface of the implanted wafer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implant the metallic species at a depth (Rp) of between 5 nm

and 20 nm under the surface of the implanted wafer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. See MPEP § 2144.05.

Re claims 11 and 37, Kub et al disclose at least one of the wafers (80 in FIG. 2) being thinned, before the formation step of metallic compounds (Pt). (column 5, lines 62-67, column 6, lines 66-67 and column 7, lines 1-5)

Kub et al fail to disclose at least one of the wafers being thinned, after assembly or after the formation step of metallic compounds.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have at least one of the wafers being thinned, after assembly or after the formation step of metallic compounds since the selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946); *In re Gibson*, 39 F.2d 975, 5 USPQ 230 (CCPA 1930). See MPEP § 2144.04.

8. Claims 4 and 30; 53-54 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kub et al in view of Pike, Jr. et al (5,528,058).

Re claims 4 and 30, Kub et al disclose implanting the metallic species (lifetime killing Pt 92 in FIG. 2; column 6, lines 66-67 and column 7, lines 1-5)

Kub et al fail to disclose the metallic species being implanted at a dose of between 10^{14} and a few 10^{18} species/cm^2.

Pike, Jr. et al disclose in FIG. 15 a metallic species (Pt 69) being implanted at a dose of between 10^{11} and a few 10^{16} species/cm^2. (column 21; lines 42-67)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the metallic implantation species parameters of Pike, Jr. et al with the method of Kub et al to effect lifetime control of devices. (Pike, Jr. et al)

Re claim 53, Kub et al disclose in FIGS. 1-9 a sealing processing for two wafers made of semiconducting materials, comprising:

-a step for implantation of metallic species (lifetime killing Pt 92 in FIG. 2; column 6, lines 66-67 and column 7, lines 1-5) in at least the first wafer, at a depth (Rp) of 10 microns (column 2, lines 65-67, column 3, lines 1-8, column 6, lines 66-67 and column 7, lines 1-5) under the surface of said first wafer (80 in FIG. 2; column 6, lines 66-67 and column 7, lines 1-5),

- a step for assembly of the first and second wafer (95 in FIG. 6; column 9, lines 23-61) by molecular (hydrophobic) bonding (column 9, lines 37-61),

- a step for formation of metallic compounds (PtSi interface 103 in FIG. 6; column 9, lines 32-37), alloys between the implanted metallic species and the semiconducting materials of the two wafers (after the two wafers are bonded, they are annealed which in turn causes the Pt metallic species to diffuse and react with the silicon substrate (wafer) to form the metallic compound PtSi; column 6, lines 66-67 and column 7, lines 1-5 and 53-60), said metallic compound forming a resistive contact between the two wafers, at the assembly interface (FIGS. 7-9; column 9, lines 62-67 and column 10, lines 1-25).

Kub et al fail to disclose the metallic species being implanted at a depth (Rp) of between 5 nm and 20 nm under the surface of the implanted wafer; and at a dose of between 10^{14} and a few 10^{18} species/cm^2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implant the metallic species at a depth (Rp) of between 5 nm and 20 nm under the surface of the implanted wafer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. See MPEP § 2144.05.

Pike, Jr. et al disclose in FIG. 15 a metallic species (Pt 69) being implanted at a dose of between 10^{11} and a few 10^{16} species/cm^2. (column 21; lines 42-67)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the metallic implantation species parameters of Pike, Jr. et al with the method of Kub et al to effect lifetime control of devices. (Pike, Jr. et al)

Re claim 54, Kub et al disclose the formation step of the metallic compounds resulting from a heat treatment at a temperature equal at least to the formation temperature of the said compounds. (800° C or less; column 6, lines 66-67 and column 7, lines 1-5 and 53-60)

9. Claims 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kub et al and Pike, Jr. et al as applied to claim 53 above, and further in view of Kish, Jr. et al (5,783,477) and Abe et al (US 2002/0157790 A1).

Re claims 55-57, Kub et al and Pike, Jr. et al fail to disclose an amorphisation step before assembly to make all or part of the surface layer of the first wafer amorphous; and the amorphisation step comprising deposition of an amorphous material layer before and/or after implantation of metallic species; and the amorphisation step comprising a surface implantation, for example by hydrogen or metallic species.

Kish, Jr. et al disclose in FIG. 9 an amorphisation step before assembly to make all or part of the surface layer (93 or 95; column 8, lines 18-37) of the first wafer (semiconductor layer under 93 or 95) amorphous; and the amorphisation step comprising deposition of an amorphous material layer (91; column 8, lines 18-37); and the amorphisation step comprising a surface implantation (column 8, lines 18-37).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the amorphisation step before assembly to make all or part of the surface layer of the first wafer amorphous; and the amorphisation step comprising deposition of an amorphous material layer; and the amorphisation step comprising a surface implantation of Kish, Jr. et al with the method of Kub et al and Pike, Jr. et al to form an ohmic interface between unipolar semiconductor wafers. (Kish, Jr. et al Abstract)

Kub et al and Pike, Jr. et al and Kish, Jr. et al fail to disclose the amorphisation step comprising a surface implantation, for example by hydrogen or metallic species.

Abe et al disclose in FIGS. 2-3 the amorphisation step comprising a surface implantation, for example by hydrogen. (¶ [0064])

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the amorphisation step comprising a surface implantation, for example by hydrogen of Abe et al with the method of Kub et al and Pike, Jr. et al and Kish, Jr. et al to produce bonded wafers comprising an ion implantation of hydrogen without causing breakage of the wafers. (Abe et al Abstract)

10. Claims 5-7 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kub et al in view of Kish, Jr. et al (5,783,477) and Abe et al (US 2002/0157790 A1).

Re claims 5-7 and 31-33, Kub et al fail to disclose an amorphisation step before assembly to make all or part of the surface layer of the first wafer amorphous; and the amorphisation step comprising deposition of an amorphous material layer before and/or after implantation of metallic species; and the amorphisation step comprising a surface implantation, for example by hydrogen or metallic species.

Kish, Jr. et al disclose in FIG. 9 an amorphisation step before assembly to make all or part of the surface layer (93 or 95; column 8, lines 18-37) of the first wafer (semiconductor layer under 93 or 95) amorphous; and the amorphisation step comprising deposition of an amorphous material layer (91; column 8, lines 18-37); and the amorphisation step comprising a surface implantation (column 8, lines 18-37).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the amorphisation step before assembly to make all or part of the surface layer of the first wafer amorphous; and the amorphisation step comprising deposition of an amorphous material layer; and the amorphisation step comprising a

surface implantation of Kish, Jr. et al with the method of Kub et al to form an ohmic interface between unipolar semiconductor wafers. (Kish, Jr. et al Abstract)

Kub et al and Kish, Jr. et al fail to disclose the amorphisation step comprising a surface implantation, for example by hydrogen or metallic species.

Abe et al disclose in FIGS. 2-3 the amorphisation step comprising a surface implantation, for example by hydrogen. (¶ [0064])

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the amorphisation step comprising a surface implantation, for example by hydrogen of Abe et al with the method of Kub et al and Kish, Jr. et al to produce bonded wafers comprising an ion implantation of hydrogen without causing breakage of the wafers. (Abe et al Abstract)

11. Claims 13-14 and 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kub et al in view of Yu et al (US 6,410,371 B1).

Re claims 13-14 and 39-40, Kub et al fail to disclose at least one of the wafers comprising a weakening plane; and the wafer comprising a weakening plane being "thinned by fracture along the said weakening plane, after assembly or after the formation step of the metallic compounds.

Yu et al disclose in FIGS. 2 and 3A-3F at least one of the wafers (64 in FIG. 3E) comprising a weakening plane (weak zone); and the wafer comprising a weakening plane being thinned by fracture (broken) along the said weakening plane. (column 4, lines 19-43)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute the at least one of the wafers comprising a weakening plane of Yu et al for one of the wafers of Kub et al; and to use the wafer comprising a weakening plane being thinned by fracture along the said weakening plane of Yu et al with the method of Kub et al to form a semiconductor-on-insulator (SOI) wafer. (Yu et al Abstract)

12. Claims 17 and 19; and 43 and 45 rejected under 35 U.S.C. 103(a) as being unpatentable over Kub et al in view of Abe et al.

Re claims 17 and 43, Kub et al fail to disclose the formation of an insulating layer on the first wafer, before it is implanted with metallic species.

Abe et al disclose the formation of an insulating layer (silicon oxide) on the first wafer, before it is implanted with hydrogen. (¶ [0044])

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the formation of an insulating layer (silicon oxide) on the first wafer, before it is implanted of Abe et al with the method of Kub et al to produce bonded wafers without causing breakage of the wafers. (Abe et al Abstract)

Re claims 19 and 45, Kub et al disclose the implantation step of metallic species (Pt lifetime killing) being done through a mask (photolithographic or metal) to obtain local implantation zones (column 7, lines 9-20).

Kub et al fail to disclose the first wafer comprising at least one insulating zone located at the surface so as to obtain local implantation zones.

Abe et al disclose the formation of an insulating layer (silicon oxide) on the first wafer, before it is implanted with hydrogen. (¶ [0044])

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the formation of an insulating layer (silicon oxide) on the first wafer, before it is implanted of Abe et al with the method of Kub et al as discussed above for claims 17 and 43.

Further, It would have been obvious to one having ordinary skill in the art at the time the invention was made that if the formation of an insulating layer (silicon oxide) on the first wafer of Abe et al were used with the method of Kub et al to form local implantation zones, the insulation layer would be patterned by the photolithographic mask as well, thus creating at least one insulating zone located at the surface so as to obtain local implantation zones.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC W. JONES whose telephone number is (571)270-3416. The examiner can normally be reached on Monday-Friday 5:30AM-3:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571)272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892

/ERIC W JONES/
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1/7/2009